Abstract

A turbo code providing very low error rate performance and which can be practically implemented on an integrated circuit is described. In accordance with one embodiment of the invention a turbo code is comprised of three constituent codes and two interleavers placed in parallel concatenated configuration. In a first exemplary embodiment of the invention, the constituent codes are configured with at least one higher rate code and at least one lower rate code. In a second embodiment of the invention, the code is configured with one higher rate code and two lower rate codes. In a third embodiment of the invention, the code is comprised of at least one higher depth constituent code and at least one lower depth constituent code. In a fourth embodiment of the invention, the code is comprised of at least one higher rate and higher depth constituent code.